

Configuring Frequency Synchronization

Frequency Synchronization is used to distribute precision frequency around a network. Frequency is synchronized accurately using Synchronized Ethernet (SyncE) in devices connected by Ethernet in a network.

This module describes the concepts around this and details the various configurations involved. For information on SyncE commands, see *System Management Command Reference for Cisco ASR 9000 Series Routers*.

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Overview

Frequency or timing synchronization is the ability to distribute precision frequency around a network. In this context, timing refers to precision frequency, not an accurate time of day. Precision frequency is required in next generation networks for applications such as circuit emulation.

To achieve compliance to ITU specifications for TDM, differential method circuit emulation must be used, which requires a known, common precision frequency reference at each end of the emulated circuit. The incumbent example of frequency synchronization is provided by SDH equipment. This is used in conjunction with an external timing technology to provide synchronization of precision timing across the network.

SDH equipments are widely replaced by Ethernet equipments and synchronized frequency is required over such Ethernet ports. Synchronous Ethernet (SyncE) is used to accurately synchronize frequency in devices connected by Ethernet in a network. SyncE provides level frequency distribution of known common precision frequency references to a physical layer Ethernet network.

To maintain SyncE links, a set of operational messages are required. These messages ensure that a node is always deriving timing information from the most reliable source and then transfers the timing source quality information to clock the SyncE link. In SDH networks, these are known as Synchronization Status Messages (SSMs). SyncE uses Ethernet Synchronization Message Channel (ESMC) to provide transport for SSMs.

Source and Selection Points

Frequency Synchronization implementation involves Sources and Selection Points.

A Source inputs frequency signals into a system or transmits them out of a system. There are four types of sources:

- Line interfaces. This includes SyncE interfaces and SONET interfaces.
- Clock interfaces. These are external connectors for connecting other timing signals, such as BITS, UTI and GPS.
- PTP clock. If IEEE 1588 version 2 is configured on the router, a PTP clock may be available to frequency synchronization as a source of the time-of-day and frequency.
- Internal oscillator. This is a free-running internal oscillator chip.

Each source has a Quality Level (QL) associated with it which gives the accuracy of the clock. This QL information is transmitted across the network using ESMC or SSMs contained in the SDH frames. This provides information about the best available source the devices in the system can synchronize to. To define a predefined network synchronization flow and prevent timing loops, you can assign priority values to the sources on each router. The combination of QL information and user-assigned priority levels allow each router to choose a source to synchronize its SyncE or SDH interfaces, as described in the ITU standard G.781.

A Selection Point is any point where a choice is made between several frequency signals and possibly one or many of them are selected. Selection points form a graph representing the flow of timing signals between different cards in a router running Cisco IOS XR software. For example, there can be one or many selection points between different Synchronous Ethernet inputs available on a single line card. This information is forwarded to a selection point on the RSP, to choose between the selected source from each card.

The input signals to the selection points can be:

- Received directly from a source.
- Received as the output from another selection point on the same card.
- Received as the output from a selection point on a different card.

The output of a selection point can be used in a number of ways, like:

- To drive the signals sent out of a set of interfaces.
- As input into another selection point on a card.
- As input into a selection point on an another card.

Use **show frequency synchronization selection** command to see a detailed view of the different selection points within the system.



Note

- We recommend you to configure, and enable Frequency Synchronization selection input on two interfaces per line card.
- For link aggregation, you must configure and enable Frequency Synchronization selecction input on a single bundle member.

SyncE Hardware Support Matrix

This table provides details on the harware that supports SyncE:

Note The table also contains support details of upcoming releases. You can read this table in context of the current release and see relevant *Release Notes* for more information on supported features and hardware.

Table 1: Feature History Table

Feature Name	Release Information	Feature Description
SyncE Support on ASR 9000 5th Generation 400G Ethernet Line Card	Release 25.2.1	Frequency Synchronization is now supported on the following line card: • A99-4HG-FLEX-X-SE Route Processor: • A9K-RSP5-X-SE/TR • A9K-RSP5-SE/TR • A99-RP3-X-SE/TR • A99-RP3-SE/TR
SyncE Support on ASR 9000 5th Generation 400G Ethernet Line Card	Release 25.1.1	Frequency Synchronization is now supported on the following line card: • A9K-4HG-FLEX-X-SE Route Processor: • A9K-RSP5-X-SE • A9K-RSP5-X-TR
SyncE Support on 5th Generation 10-Port 400 Gigabit Ethernet Line Cards: • A99-10X400GE-X-SE • A99-10X400GE-X-TR	Release 7.3.2	Frequency Synchronization is used to distribute precision frequency around a network. Frequency is synchronized accurately using Synchronized Ethernet (SyncE) in devices connected by Ethernet in a network. SyncE is now supported on the line cards: • A99-10X400GE-X-SE • A99-10X400GE-X-TR

Hardware Variant	Cisco IOS XR	Cisco IOS XR 64 bit
A9K-8X100GE-L-SE/TR (10GE and 100GE)	5.3.0	6.1.1
A9K-RSP880-SE/TR	5.3.0	6.1.1
A9K-8X100GE-L-SE/TR (40-GE)	6.0.1	6.1.1
A9K-4X100GE-SE/TR A9K-8X100GE-SE/TR	5.3.2 (100G LAN only) 6.0.1	6.1.1
A9K-MOD400-SE/TR A9K-MOD200-SE/TR with MPA 20x10GE and Legacy MPAs	6.0.1	6.2.2
A9K-MOD400-SE/TR A9K-MOD200-SE/TR with MPAs 2x100 and 1x100	6.1.3	6.2.2
A9K-400G-DWDM-TR	5.3.3 6.0.1	
A9K-24X10GE-1G-SE/TR A9K-48X10GE-1G-SE/TR	6.2.1	6.3.2
A99-RSP-SE/TR (Cisco ASR 9910 Series Routers)	6.1.4	6.3.2
RSP880-LT-SE/TR	6.2.2	6.4.1
A9K-RSP440-TR/SE Enhanced Ethernet Linecards A99-RP-SE	4.3.4	
A99-RP2-TR/SE	5.3.0	6.3.2 6.4.1
Cisco ASR 9001 Series Routers	4.3.4	
Cisco ASR 9901 Series Routers	NA	6.4.1
A99-RSP-SE/TR (Cisco ASR 9906 Series Routers)	6.3.1	6.3.2
A9K-RSP5-SE/TR	NA	6.5.15
A99-RP3-SE/TR	NA	6.5.15
A9K-8X100GE-X-TR	NA	6.5.15

Hardware Variant	Cisco IOS XR	Cisco IOS XR 64 bit
A9K-16X100GE-TR	NA	6.5.15
A9K-32X100GE-TR	NA	6.5.15
A99-32X100GE-X-TR	NA	7.1.15
A9K-8HG-FLEX-SE/TR	NA	7.1.15
A9K-20HG-FLEX-SE/TR	NA	7.1.15
ASR-9903	NA	7.1.3
A9903-20HG-PEC	NA	7.1.3
A99-10X400GE-X-SE/TR	NA	7.3.2
A99-12X100GE	NA	7.4.1
A9K-4X100GE	NA	7.4.1
ASR-9902	NA	7.4.1
A9K-4HG-FLEX-SE/TR	NA	7.4.1
A99-4HG-FLEX-SE/TR	NA	7.4.1
A9K-4HG-FLEX-X-SE	NA	25.1.1
A99-4HG-FLEX-X-SE	NA	25.2.1

SyncE Restrictions

This section lists a few restrictions in configuring frequency synchronization. They are:

- On SyncE line interfaces, you can configure multiple interfaces for SyncE input. However, only one interface from each PHY gets selected as best source and programmed as SyncE input (there is no restriction on SyncE output) on the A9K-24X10GE-1G-SE/TR and A9K-48X10GE-1G-SE/TR line cards.
- *clock-interface timing-mode independent* configuration is not supported on Cisco A9K-RSP5-X-TR, A9K-RSP5-X-SE, A99-RP3-X-TR and A99-RP3-X-SE.

SyncE and extended ESMC

The Ethernet Synchronization Message Channel (ESMC) protocol is specified in the ITU-T G.8262.1. It enables frequency synchronization across a network over Ethernet ports with the ability to select enhanced quality levels. Enhanced quality levels lead to improved bandwidth, frequency accuracy, and holdover along with reduced noise generation in a network.

Table 2: Feature History Table

Feature name	Release Information	Feature Description
SyncE and extended ESMC	Release 25.2.1	ITU-T G.8262.1 recommendation defines the requirements for timing devices used in synchronizing network equipment. For example, bandwidth, frequency accuracy, holdover, and noise generation. With enhanced SyncE (eSyncE) and extended ESMC (eESMC) support, the routers are capable of handling the following SyncE clocks on the network: • Enhanced Primary Reference Clock (ePRC) • Enhanced Primary Reference Timing Clock (ePRTC)

As part of the ESMC protocol, Synchronization Status Messages (SSMs) distributes the Quality Level (QL) of timing signals. The updated G.8262.1 standard provides a new and enhanced Quality Level (QL) of Type Length Value (TLV) that allows more precise quality to provide accurate clocks.

The new and enhanced QL of TLV that is part of the updated G.8262.1 standard is known as **enhanced SyncE (eSyncE)**. The enhanced QL of TLV enables support for more QL values. You can configure a router to send or receive the enhanced TLV. The enhanced QL of TLV results in more precise synchronization of clocks across a network.

Restrictions of extended ESMC

These restrictions must be observed on the routers for usage of extended ESMC:

- Router that do not support eSyncE do not support extended ESMC.
- Router that does not support eSyncE ignores any enhanced TLVs it receives and hence does not support enhanced quality to provide accurate clocks.
- Router that does not support eSyncE at ingress nodes drop the QL TLV received from the previous node supporting eSyncE.
- The extended QL TLV is newly applied only at the subsequent node that supports enhanced ESMC.

Clocking Support for nV Cluster

ASR9K cluster consists of two chassis connected together to provide redundancy and to meet higher bandwidth requirements. RSP440 provides two ICS (Inter-Chassis Synchronization) interfaces on the front plate. Clocking functionality support is added to the ICS interfaces. The ICS interfaces could be used for clocking, in the

absence of other methods to synchronize frequency and Time-of-day information between the two cluster racks

nV Cluster Limitations

The limitations for the frequency synchronization support for cluster are:

- This feature is supported only on RSP440.
- The two chassis of the cluster have to be co-located. The length of the cable used for the ICS link should be less than 10 meters. This is needed to ensure the phase delay added due the length of the cable is within limits.
- SSM and QL is not supported on ICS links. SSM messages are not exchanged over the ICS interface. Hence, QL value needs to be configured under ICS clock interface configuration.
- The selection of an input clock source is based on the configuration of priority, QL as well as the clock quality. For SyncE, the ICS interfaces are similar to the SyncE line interfaces as far as input clock selection is concerned.
- All Input clock sources to cluster setup has to be redundant.
- No support for 1588 BC on LAG interfaces with member links across racks.

Inter-Chassis Synchronization (ICS)

ICS-Frequency Synchronization

Frequency synchronization is provided using Inter-Chassis Synchronization links (ICS). These are dedicated interfaces on the RSP used to synchronize the time and frequency.

The ICS link between the Primary DSC and Backup DSC carries the clock. There is no transfer of QL information from Primary DSC to Backup DSC.The clock direction is always from Primary DSC to Backup DSC. The Primary DSC transmits the clock and Backup DSC receives the clock.

The ICS clock interface (sync 2 or sync 3) is a clock input on the Backup DSC. The clock selection algorithm for SyncE is independent on each RSP. So, output clock from the rack which has Primary DSC is the outcome of the clock selection on the Primary DSC. The output clock from the rack which has Backup DSC is the outcome of the clock selection on the Backup DSC. If the ICS clock interface configuration is such that it is the selected clock on the Backup DSC, then the output clocks from the Primary rack and Backup rack are synchronised.

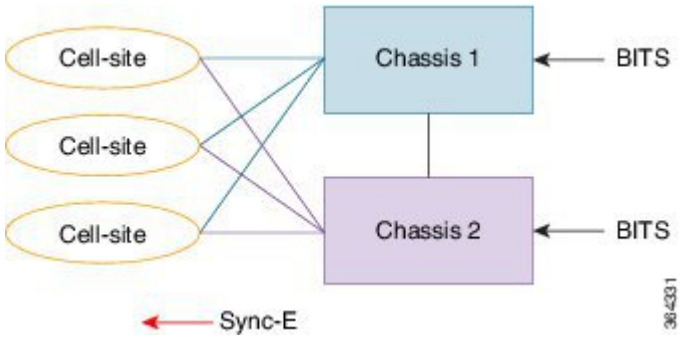
ICS-Time-of-Day

The ICS links also carry Time of Day (ToD) information when the ICS clock interfaces are configured for the same. Only the Backup DSC can synchronise with ToD from the Primary DSC and not vice versa. The 1588 clock information transmitted on all 1588 interfaces in the cluster (including interfaces on Backup rack) is of the clock selected at the Primary DSC. Thus, it is important that ICS clock interface on Backup DSC is configured such that it is the clock which is selected for ToD on the Backup DSC.

Recommended ICS Interface Connections

No inter-chassis frequency or time synchronization support:

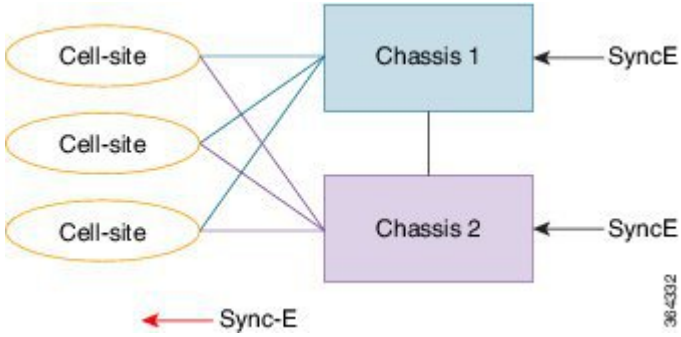
Figure 1: No inter-chassis frequency support



SyncE is used from the ASR9K cluster to provide precision frequency to mobile cell sites. A BITS clock is connected to each chassis of the cluster, meaning that the frequencies of both chassis are synchronized and the cell sites will all be synchronized, regardless of which chassis they synchronize to. In most deployments redundant BITS connections would be made to each chassis, to prevent against failure of any single BITS link.

With inter-chassis synchronization support:

Figure 2: With inter-chassis synchronization support



SyncE is used to synchronize the frequency of an ASR9k cluster to an upstream device. To provide redundancy in the case of one of the external SyncE inputs going down, the frequencies of the different cluster chassis must somehow be synchronized; else cell sites which select links from different chassis to synchronize may be out of sync if one of the SyncE links goes down.

Configuring Frequency Synchronization

Enabling Frequency Synchronization on the Router

This task describes the router-level configuration required to enable frequency synchronization.

Important **Frequency synchronization** configuration is mandatory to enable any type of frequency or time source on the router. This includes SyncE, clock-interfaces, Precision Time Protocol (PTP) or internal oscillator.

Note If timing mode system is not configured, the major alarm `T4 PLL is in FREERUN mode` is raised. This alarm has no functional impact to the system behavior.

SUMMARY STEPS

1. **configure**
2. **frequency synchronization**
3. **clock-interface timing-mode** {**independent** | **system**
4. **quality itu-t option** {**1** | **2 generation** {**1** | **2**}}
5. **log selection** {**changes** | **errors**}
6. Use one of these commands:
   - **end**
   - **commit**

DETAILED STEPS

Procedure

	Command or Action	Purpose
Step 1	**configure** **Example:** `RP/0/RSP0/CPU0:router# configure`	Enters global configuration mode.
Step 2	**frequency synchronization** **Example:** `RP/0/RSP0/CPU0:router(config)# frequency synchronization`	Enables frequency synchronization on the router.
Step 3	**clock-interface timing-mode** {**independent**	**system** **Example:** `RP/0/RSP0/CPU0:router(config-freqsync)# clock-interface timing-mode system`	Configures the type of timing sources that can be used to drive the output from a clock interface. If this command is not used, the default quality mode is used. In the default mode, the clock interface output is driven only by input from line interfaces and the internal oscillator; it is never driven by input from another clock interface. In addition, some heuristic tests are run to detect if the signal being sent out of one clock interface can be looped back by some external box and sent back in via the same, or another clock interface. • **independent**—Specifies that the output of clock interfaces is driven only by the line interfaces (SyncE and SONET/SDH), as in the default mode. Loopback detection is disabled.

	Command or Action	Purpose
		• **system**—Specifies that the output of a clock interface is driven by the system-selected timing source (the source used to drive all SyncE and SONET/SDH interfaces), including clock interfaces. Loopback detection is disabled.

Step 4	**quality itu-t option** {**1** | **2 generation** {**1** | **2**}}
	Example:
	`RP/0/RSP0/CPU0:router(config-freqsync)# quality itu-t`
	`option 2 generation 1`
		(Optional) Specifies the quality level for the router. The default is **option 1**.
		• **option 1**—Includes PRC, SSU-A, SSU-B, SEC and DNU.
		• **option 2 generation 1**—Includes PRS, STU, ST2, ST3, SMC, ST4, RES and DUS.
		• **option 2 generation 2**—Includes PRS, STU, ST2, ST3, TNC, ST3E, SMC, ST4, PROV and DUS.
		Note
		The quality option configured here must match the quality option specified in the **quality receive** and **quality transmit** commands in interface frequency synchronization configuration mode.

Step 5	**log selection** {**changes** | **errors**} **Example:** `RP/0/RSP0/CPU0:router(config-freqsync)# log selection changes`	Enables logging to frequency synchronization. • **changes**—Logs every time there is a change to the selected source, in addition to errors. • **errors**—Logs only when there are no available frequency sources, or when the only available frequency source is the internal oscillator.

Step 6	Use one of these commands:
	• **end**
	• **commit**
	Example:
	`RP/0/RSP0/CPU0:router(config-freqsync)# end`
	or
	`RP/0/RSP0/CPU0:router(config-freqsync)# commit`
		Saves configuration changes.
		• When you issue the **end** command, the system prompts you to commit changes:
		`Uncommitted changes found, commit them before exiting(yes/no/cancel)? [cancel]:`
		• Entering **yes** saves configuration changes to the running configuration file, exits the configuration session, and returns the router to EXEC mode.
		• Entering **no** exits the configuration session and returns the router to EXEC mode without committing the configuration changes.
		• Entering **cancel** leaves the router in the current configuration session without exiting or committing the configuration changes.

	Command or Action	Purpose
		• Use the **commit** command to save the configuration changes to the running configuration file, and remain within the configuration session.

What to do next

Configure frequency synchronization on any interfaces that should participate in frequency synchronization.

Configuring Frequency Synchronization on an Interface

By default, there is no frequency synchronization on line interfaces. Use this task to configure an interface to participate in frequency synchronization.

Before you begin

You must enable frequency synchronization globally on the router.

SUMMARY STEPS

1. **configure**
2. **interface** *type interface-path-id*
3. **frequency synchronization**
4. **selection input**
5. **priority** *priority-value*
6. **wait-to-restore** *minutes*
7. **ssm disable**
8. **time-of-day-priority** *priority*
9. **quality transmit** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option*
10. **quality receive** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option*
11. Use one of these commands:
    - **end**
    - **commit**

DETAILED STEPS

Procedure

	Command or Action	Purpose
Step 1	**configure** **Example:** `RP/0/RSP0/CPU0:router# configure`	Enters global configuration mode.

	Command or Action	Purpose
Step 2	**interface** *type interface-path-id* **Example:** `RP/0/RSP0/CPU0:router(config)# interface GigabitEthernet0/1/1/0`	Enters interface configuration mode.
Step 3	**frequency synchronization** **Example:** `RP/0/RSP0/CPU0:router(config-if)# frequency synchronization`	Enables frequency synchronization on the interface and enters interface frequency synchronization mode to configure the various options. By default, this causes the system selected frequency signal to be used for clocking transmission, but does not enable the use of the interface as an input.
Step 4	**selection input** **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# selection input`	(Optional) Specifies the interface as a timing source to be passed to the selection algorithm.
Step 5	**priority** *priority-value* **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# priority 100`	(Optional) Configures the priority of the frequency source on a controller or an interface. Values can range from 1 (highest priority) to 254 (lowest priority). The default value is 100. This command is used to set the priority for an interface or clock interface. The priority is used in the clock-selection algorithm to choose between two sources that have the same quality level (QL). Lower priority values are preferred.
Step 6	**wait-to-restore** *minutes* **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# wait-to-restore 300`	(Optional) Configures the wait-to-restore time, in minutes, for frequency synchronization on an interface. This is the amount of time after the interface comes up before it is used for synchronization. Values can range from 0 to 12. The default value is 5.
Step 7	**ssm disable** **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# ssm disable`	(Optional) Disables Synchronization Status Messages (SSMs) on the interface. • For SyncE interfaces, this disables sending ESMC packets, and ignores any received ESMC packets. • For SONET and clock interfaces, this causes DNUs to be sent, and ignores any received QL value.
Step 8	**time-of-day-priority** *priority* **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# time-of-day-priority 50`	(Optional) Specifies the priority of this time source as the time-of-day (ToD) source. The priority is used as the first criterion when selecting between sources for a time-of-day selection point. Values can range from 1 (highest priority) to 254 (lowest priority); the default value is 100.
Step 9	**quality transmit** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option*	(Optional) Adjusts the QL that is transmitted in SSMs.

	Command or Action	Purpose
	Example: `RP/0/RSP0/CPU0:router(config-clk-freqsync)# quality transmit highest itu-t option 1 prc`	• **exact** *ql*—Specifies the exact QL to send, unless DNU would otherwise be sent. • **highest** *ql*—Specifies an upper limit on the QL to be sent. If the selected source has a higher QL than the QL specified here, this QL is sent instead. • **lowest** *ql*—Specifies a lower limit on the QL to be sent. If the selected source has a lower QL than the QL specified here, DNU is sent instead. The quality option specified in this command must match the globally-configured quality option in the **quality itu-t option** command. **Note** For clock interfaces that do not support SSM, only the lowest QL can be specified. In this case, rather than sending DNU, the output is squelched, and no signal is sent.
Step 10	**quality receive** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option* **Example:** `RP/0/RSP0/CPU0:router(config-clk-freqsync)# quality receive highest itu-t option 1 prc`	(Optional) Adjusts the QL value that is received in SSMs, before it is used in the selection algorithm. • **exact** *ql*—Specifies the exact QL regardless of the value received, unless the received value is DNU. • **highest** *ql*—Specifies an upper limit on the received QL. If the received value is higher than this specified QL, this QL is used instead. • **lowest** *ql*—Specifies a lower limit on the received QL. If the received value is lower than this specified QL, DNU is used instead. The quality option specified in this command must match the globally-configured quality option in the **quality itu-t option** command. **Note** For clock interfaces that do not support SSM, only the exact QL can be specified.
Step 11	Use one of these commands: • **end** • **commit** **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# end` or	Saves configuration changes. • When you issue the **end** command, the system prompts you to commit changes: `Uncommitted changes found, commit them before exiting(yes/no/cancel)? [cancel]:` • Entering **yes** saves configuration changes to the running configuration file, exits the

	Command or Action	Purpose
	`RP/0/RSP0/CPU0:router(config-if-freqsync)# commit`	configuration session, and returns the router to EXEC mode. • Entering **no** exits the configuration session and returns the router to EXEC mode without committing the configuration changes. • Entering **cancel** leaves the router in the current configuration session without exiting or committing the configuration changes. • Use the **commit** command to save the configuration changes to the running configuration file, and remain within the configuration session.

Configuring Frequency Synchronization on a Clock Interface

To enable a clock interface to be used as frequency input or output, you must configure the port parameters and frequency synchronization, as described in this task.

Note The configuration on clock interfaces must be the same for corresponding clock interfaces across all RSPs to avoid changes in frequency synchronization behavior in the event of an RSP switchover.

SUMMARY STEPS

1. **configure**
2. **clock-interface sync** *port-no* **location** *node-id*
3. **port-parameters** {**bits-input** *mode* | **bits-output** *mode* | **dti**}
4. **ics**
5. **frequency synchronization**
6. **selection input**
7. **priority** *priority-value*
8. **wait-to-restore** *minutes*
9. **ssm disable**
10. **time-of-day-priority** *priority*
11. **quality transmit** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option*
12. **quality receive** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option*
13. Use one of these commands:
    - **end**
    - **commit**

DETAILED STEPS

Procedure

	Command or Action	Purpose
Step 1	**configure** **Example:** `RP/0/RSP0/CPU0:router# configure`	Enters global configuration mode.
Step 2	**clock-interface sync** *port-no* **location** *node-id* **Example:** `RP/0/RSP0/CPU0:router(config)# clock-interface sync 2 location 0/2/0`	Enters clock interface configuration mode to configure the clock interface.
Step 3	**port-parameters** {**bits-input** *mode* | **bits-output** *mode* | **dti**} **Example:** `RP/0/RSP0/CPU0:router(config-clock-if)# port-parameters dti`	Specifies the type of external clock source for the clock interface. Options are BITS RX, BITS TX or DTI. The possible *mode* values for BITS interfaces are **2m**, **6m-output-only**, **e1** or **t1**.
Step 4	**ics** **Example:** `RP/0/RSP0/CPU0:router(config)# ics`	Enables chassis synchronization.

Step 5	**frequency synchronization**
	Example:
	`RP/0/RSP0/CPU0:router(config-clock-if)# frequency synchronization`
	`RP/0/RSP0/CPU0:router(config-clk-freqsync)#`
		Enters clock interface frequency synchronization mode to configure frequency synchronization parameters.
		Note
		The remaining steps in this task are the same as those used to configure the interface frequency synchronization.

Step 6	**selection input** **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# selection input`	(Optional) Specifies the interface as a timing source to be passed to the selection algorithm.
Step 7	**priority** *priority-value* **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# priority 100`	(Optional) Configures the priority of the frequency source on a controller or an interface. Values can range from 1 (highest priority) to 254 (lowest priority). The default value is 100. This command is used to set the priority for an interface or clock interface. The priority is used in the clock-selection algorithm to choose between two sources that have the same quality level (QL). Lower priority values are preferred.

	Command or Action	Purpose
Step 8	**wait-to-restore** *minutes* **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# wait-to-restore 300`	(Optional) Configures the wait-to-restore time, in minutes, for frequency synchronization on an interface. This is the amount of time after the interface comes up before it is used for synchronization. Values can range from 0 to 12. The default value is 5.
Step 9	**ssm disable** **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# ssm disable`	(Optional) Disables Synchronization Status Messages (SSMs) on the interface. • For SyncE interfaces, this disables sending ESMC packets, and ignores any received ESMC packets. • For SONET and clock interfaces, this causes DNUs to be sent, and ignores any received QL value.
Step 10	**time-of-day-priority** *priority* **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# time-of-day-priority 50`	(Optional) Specifies the priority of this time source as the time-of-day (ToD) source. The priority is used as the first criterion when selecting between sources for a time-of-day selection point. Values can range from 1 (highest priority) to 254 (lowest priority); the default value is 100.
Step 11	**quality transmit** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option* **Example:** `RP/0/RSP0/CPU0:router(config-clk-freqsync)# quality transmit highest itu-t option 1 prc`	(Optional) Adjusts the QL that is transmitted in SSMs. • **exact** *ql*—Specifies the exact QL to send, unless DNU would otherwise be sent. • **highest** *ql*—Specifies an upper limit on the QL to be sent. If the selected source has a higher QL than the QL specified here, this QL is sent instead. • **lowest** *ql*—Specifies a lower limit on the QL to be sent. If the selected source has a lower QL than the QL specified here, DNU is sent instead. The quality option specified in this command must match the globally-configured quality option in the **quality itu-t option** command. **Note** For clock interfaces that do not support SSM, only the lowest QL can be specified. In this case, rather than sending DNU, the output is squelched, and no signal is sent.
Step 12	**quality receive** {**exact** | **highest** | **lowest**} **itu-t option** *ql-option* **Example:** `RP/0/RSP0/CPU0:router(config-clk-freqsync)# quality receive highest itu-t option 1 prc`	(Optional) Adjusts the QL value that is received in SSMs, before it is used in the selection algorithm. • **exact** *ql*—Specifies the exact QL regardless of the value received, unless the received value is DNU. • **highest** *ql*—Specifies an upper limit on the received QL. If the received value is higher than this specified QL, this QL is used instead.

	Command or Action	Purpose
		• **lowest** *ql*—Specifies a lower limit on the received QL. If the received value is lower than this specified QL, DNU is used instead. The quality option specified in this command must match the globally-configured quality option in the **quality itu-t option** command. **Note** For clock interfaces that do not support SSM, only the exact QL can be specified.

Step 13	Use one of these commands:
	• **end**
	• **commit**
	Example:
	`RP/0/RSP0/CPU0:router(config-if-freqsync)# end`
	or
	`RP/0/RSP0/CPU0:router(config-if-freqsync)# commit`
		Saves configuration changes.
		• When you issue the **end** command, the system prompts you to commit changes:
		`Uncommitted changes found, commit them before exiting(yes/no/cancel)? [cancel]:`
		• Entering **yes** saves configuration changes to the running configuration file, exits the configuration session, and returns the router to EXEC mode.
		• Entering **no** exits the configuration session and returns the router to EXEC mode without committing the configuration changes.
		• Entering **cancel** leaves the router in the current configuration session without exiting or committing the configuration changes.
		• Use the **commit** command to save the configuration changes to the running configuration file, and remain within the configuration session.

Configuring Clock Interface with DTI input

This procedure describes the steps involved to configure a Clock interface with DTI input.

1. To configure a clock interface, use **clock-interface sync** *value* **location** *node* command in the configuration mode.

```
RP/0/RSP0/CPU0:router(config)# clock-interface sync 1 location 0/RSP0/CPU0
```

2. To configure port parameters for the given clock interface, use **port-parameters dti** command in the clock-interface configuration mode.

```
RP/0/RSP0/CPU0:router(config-clock-if)# port-parameters dti
```

3. To enable frequency synchronization, use **frequency synchronization** command in the clock-interface configuration mode.

```
RP/0/RSP0/CPU0:router(config-clock-if)# frequency synchronization
```

4. To configure selection input for the given clock interface, use **selection input** command in the frequency-synchronization clock-configuration mode.

```
RP/0/RSP0/CPU0:router(config-clk-freqsync)# selection input
```

5. To configure priority for the clock interface, use **priority** *number* command in the frequency-synchronization clock-configuration mode.

```
RP/0/RSP0/CPU0:router(config-clk-freqsync)# priority 1
```

6. To configure wait-to-restore time for the clock interface, use **wait-to-restore** *number* command in the frequency-synchronization clock-configuration mode.

```
RP/0/RSP0/CPU0:router(config-clk-freqsync)# wait-to-restore 0
```

7. To disable SSM packets for the clock interface, use **ssm disable** command in the frequency-synchronization clock-configuration mode.

```
RP/0/RSP0/CPU0:router(config-clk-freqsync)# ssm disable
```

8. To configure quality settings for the clock interface, use **quality receive exact itu-t option** *number* **generation** *number* **PRS** command in the frequency-synchronization clock-configuration mode.

```
RP/0/RSP0/CPU0:router(config-clk-freqsync)# quality receive exact itu-t option 2
generation 2 PRS
```

Verification

To display the current running configuration of an interface, use **show run clock-interface** command.

```
RP/0/RSP0/CPU0:router# show run clock-interface sync 1 location 0/RSP0/CPU0

clock-interface sync 1 location 0/RSP0/CPU0
port-parameters
  dti
!
frequency synchronization
  selection input
  priority 1
  wait-to-restore 0
  ssm disable
  quality receive exact itu-t option 2 generation 2 PRC
!
!RP/0/RSP0/CPU0:router#
```

Configuring GPS Settings for a sync2 interface

This procedure describes the steps involved to configure GPS settings for a sync2 interface.

1. To configure a clock interface, use **clock-interface sync** *port-number* **location** *interface-location* command in the configuration mode.

```
RP/0/RSP0/CPU0:router(config)# clock-interface sync 2 location 0/RSP0/CPU0
```

2. To configure port parameters for the given clock interface, use **port-parameters** command in the clock-interface configuration mode.

```
RP/0/RSP0/CPU0:router(config-clock-if)# port-parameters
```

3. To configure GPS input parameters, use **gps-input tod-format gprmc pps-input ttl** command.

```
RP/0/RSP0/CPU0:router(config-clk-parms)# gps-input tod-format
gprmc pps-input ttl
```

4. To return to the clock-interface configuration mode, use **exit** command.

```
RP/0/RSP0/CPU0:router(config-clk-parms)# exit
```

5. To enable frequency synchronization, use **frequency synchronization** command in the clock-interface configuration mode.

```
RP/0/RSP0/CPU0:router(config-clock-if)# frequency synchronization
```

6. To configure selection input for the given clock interface, use **selection input** command in the frequency-synchronization clock-configuration mode.

```
RP/0/RSP0/CPU0:router(config-clk-freqsync)# selection input
```

7. To configure priority for the clock interface, use **priority** *number* command in the frequency-synchronization clock-configuration mode.

```
RP/0/RSP0/CPU0:router(config-clk-freqsync)# priority 10
```

8. To configure wait-to-restore time for the clock interface, use **wait-to-restore** *number* command in the frequency-synchronization clock-configuration mode.

```
RP/0/RSP0/CPU0:router(config-clk-freqsync)# wait-to-restore 0
```

9. To disable SSM packets for the clock interface, use **ssm disable** command in the frequency-synchronization clock-configuration mode.

```
RP/0/RSP0/CPU0:router(config-clk-freqsync)# ssm disable
```

10. To configure quality settings for the clock interface, use **quality receive exact itu-t option** *number* **generation** *number* **PRS** command in the frequency-synchronization clock-configuration mode.

```
RP/0/RSP0/CPU0:router(config-clk-freqsync)# quality receive exact itu-t option 2
generation 2 PRS
```

Verification

To verify the configured GPS parameters , use **show run clock-interface** command.

```
RP/0/RSP0/CPU0:router# show run clock-interface sync 2 location 0/RSP0/CPU0

clock-interface sync 2 location 0/RSP0/CPU0
port-parameters
gps-input tod-format gprmc pps-input ttl
!
```

GPS ToD Support for NMEA

National Marine Electronics Associations (NMEA) 0183 is a standard protocol used by GPS receivers to transmit data and is responsible for creating a standard uniform interface for digital data exchange between different marine electronic products. NMEA provides protocol strings to send out GPS updates. GPRMC is one such NMEA string that provides exact data and time (Greenwich time), latitude, longitude, heading, and speed. Router receives GPS ToD messages in serial ASCII stream through the RS422 interface in three formats - NTP Type 4, Cisco, and GPRMC. The timing data is extracted from this stream.

Note Cisco ASR 9000 Series Routers can support ToD in NMEA or GPRMC format. Currently, this is supported only on RS422.

Note You can refer to the below support information in context of the current release and see relevant *Release Notes* for more information on supported features and hardware.

Supported hardware are:

- A9K-RSP440-SE/TR
- A9K-RSP880-SE/TR
- A99-RP2-SE/TR
- A9K-RSP880-LT-SE/TR
- A99-RSP-SE/TR

Configuring ICS

This task enables inter-chassis synchronization for interfaces.

SUMMARY STEPS

1. **configure**
2. **clock-interface sync** *port-no* **location** *node-id*
3. **port-parameters ics**
4. **frequency synchronization**
5. **selection input**
6. **priority** *priority-value*
7. **wait-to-restore** *minutes*

8. **time-of-day-priority** *priority*
9. **quality receive { exact | highest | lowest} itu-t option** *option*

DETAILED STEPS

Procedure

	Command or Action	Purpose
Step 1	**configure** **Example:** `RP/0/RSP0/CPU0:router# configure`	Enters global configuration mode.
Step 2	**clock-interface sync** *port-no* **location** *node-id* **Example:** `RP/0/RSP0/CPU0:router(config)# clock-interface sync 2 location 1/RSP0/CPU0`	Enters clock interface configuration mode to configure the clock interface.
Step 3	**port-parameters ics** **Example:** `RP/0/RSP0/CPU0:router(config-clock-if)# port-parameters ics`	Enables inter-chassis synchronization.

Step 4	**frequency synchronization**
	Example:
	`RP/0/RSP0/CPU0:router(config-clock-if)# frequency synchronization`
	`RP/0/RSP0/CPU0:router(config-clk-freqsync)#`
		Enters clock interface frequency synchronization mode to configure frequency synchronization parameters.
		Note
		The remaining steps in this task are the same as those used to configure the interface frequency synchronization.

Step 5	**selection input** **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# selection input`	(Optional) Specifies the interface as a timing source to be passed to the selection algorithm.
Step 6	**priority** *priority-value* **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# priority 100`	(Optional) Configures the priority of the frequency source on a controller or an interface. Values can range from 1 (highest priority) to 254 (lowest priority). The default value is 100. This command is used to set the priority for an interface or clock interface. The priority is used in the clock-selection algorithm to choose between two sources that have the same quality level (QL). Lower priority values are preferred.
Step 7	**wait-to-restore** *minutes* **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# wait-to-restore 300`	(Optional) Configures the wait-to-restore time, in minutes, for frequency synchronization on an interface. This is the amount of time after the interface comes up before it is used for synchronization. Values can range from 0 to 12. The default value is 5.

	Command or Action	Purpose
Step 8	**time-of-day-priority** *priority* **Example:** `RP/0/RSP0/CPU0:router(config-if-freqsync)# time-of-day-priority 50`	(Optional) Specifies the priority of this time source as the time-of-day (ToD) source. The priority is used as the first criterion when selecting between sources for a time-of-day selection point. Values can range from 1 (highest priority) to 254 (lowest priority); the default value is 100.
Step 9	**quality receive { exact | highest | lowest} itu-t option** *option* **Example:** `RP/0/RSP0/CPU0:router (config-clk-freqsync) # quality receive exact itu-t option 1 PRC`	

Verifying the Frequency Synchronization Configuration

After performing the frequency synchronization configuration tasks, use this task to check for configuration errors and verify the configuration.

SUMMARY STEPS

1. **show frequency synchronization configuration-errors**
2. **show frequency synchronization interfaces brief**
3. **show frequency synchronization interfaces** *node-id*
4. **show processes fsyncmgr location** *node-id*

DETAILED STEPS

Procedure

Step 1 **show frequency synchronization configuration-errors**

Example:

```
RP/0/RSP0/CPU0:router# show frequency synchronization configuration-errors

Node 0/2/CPU0:
==============
  interface GigabitEthernet0/2/0/0 frequency synchronization
    * Frequency synchronization is enabled on this interface, but isn't enabled globally.

  interface GigabitEthernet0/2/0/0 frequency synchronization quality transmit exact itu-t option 2
generation 1 PRS
    * The QL that is configured is from a different QL option set than is configured globally.
```

Displays any errors that are caused by inconsistencies between shared-plane (global) and local-plane (interface) configurations. There are two possible errors that can be displayed:

- Frequency Synchronization is configured on an interface (line interface or clock-interface), but is not configured globally. Refer to Enabling Frequency Synchronization on the Router, on page 8

- The QL option configured on some interface does not match the global QL option. Under an interface (line interface or clock interface), the QL option is specified using the **quality transmit** and **quality receive** commands. The value specified must match the value configured in the global **quality itu-t option** command, or match the default (option 1) if the global **quality itu-t option** command is not configured.

Once all the errors have been resolved, meaning there is no output from the command, continue to the next step.

Step 2 **show frequency synchronization interfaces brief**

Example:

```
RP/0/RSP0/CPU0:router# show frequency synchronization interfaces brief

Flags:  > - Up                D - Down              S - Assigned for selection
        d - SSM Disabled      x - Peer timed out    i - Init state

Fl  Interface                QLrcv QLuse Pri QLsnt Source
=== ======================== ===== ===== === ===== ========================
>Sx GigabitEthernet0/2/0/0   Fail  Fail  100 DNU   None
Dd  GigabitEthernet0/2/0/1   n/a   Fail  100 n/a   None

RP/0/RSP0/CPU0:router# show frequency synchronization clock-interfaces brief

Flags:  > - Up                D - Down              S - Assigned for selection
        d - SSM Disabled      s - Output squelched  L - Looped back

Node 0/0/CPU0:
==============
  Fl    Clock Interface     QLrcv  QLuse  Pri QLsnd  Source
  ===== =================== ====== ====== === ====== ========================
  >S    Sync0               PRC    Fail   100 SSU-B  Internal0 [0/0/CPU0]
  >     Sync1               SSU-A  Fail   100 SSU-B  Internal0 [0/0/CPU0]
  >S    Internal0           n/a    SSU-B  255 n/a    None

Node 0/1/CPU0:
==============
  Fl    Clock Interface     QLrcv  QLuse  Pri QLsnd  Source
  ===== =================== ====== ====== === ====== ========================
  D     Sync0               None   Fail   100 SSU-B  Internal0 [0/1/CPU0]
  D     Sync1               None   Fail   100 SSU-B  Internal0 [0/1/CPU0]
  >S    Internal0           n/a    SSU-B  255 n/a    None
```

Verifies the configuration. Note the following points:

- All line interface that have frequency synchronization configured are displayed.
- All clock interfaces and internal oscillators are displayed.
- Sources that have been nominated as inputs (in other words, have **selection input** configured) have ‘S’ in the Flags column; sources that have not been nominated as inputs do not have ‘S’ displayed.

  Note
  Internal oscillators are always eligible as inputs.

- ‘>’ or ‘D’ is displayed in the flags field as appropriate.

If any of these items are not true, continue to the next step.

Step 3 **show frequency synchronization interfaces** *node-id*

Example:

```
RP/0/RSP0/CPU0:router# show frequency synchronization interfaces GigabitEthernet0/2/0/2

Interface GigabitEthernet0/2/0/2 (shutdown)
  Assigned as input for selection
  SSM Enabled
  Input:
    Down
    Last received QL: Failed
    Effective QL:     Failed, Priority: 100
  Output:
    Selected source:    Sync0 [0/0/CPU0]
    Selected source QL: Opt-I/PRC
    Effective QL:       Opt-I/PRC
  Next selection points: LC_INGRESS

RP/0/RSP0/CPU0:router# show frequency synchronization clock-interfaces location 0/1/CPU0

Node 0/1/CPU0:
==============
  Clock interface Sync0 (Down: mode not configured)
    SSM supported and enabled
    Input:
      Down
      Last received QL: Opt-I/PRC
      Effective QL:     Failed, Priority: 100
    Output:
      Selected source:    Internal0 [0/1/CPU0]
      Selected source QL: Opt-I/SSU-B
      Effective QL:       Opt-I/SSU-B
  Next selection points: RP_SYSTEM

  Clock interface Sync1 (Down: mode not configured)
    SSM supported and enabled
    Input:
      Down
      Last received QL: Opt-I/PRC
      Effective QL:     Failed, Priority: 100
    Output:
      Selected source:    Internal0 [0/1/CPU0]
      Selected source QL: Opt-I/SSU-B
      Effective QL:       Opt-I/SSU-B
  Next selection points: RP_SYSTEM

  Clock interface Internal0 (Up)
    Assigned as input for selection
    Input:
      Default QL:   Opt-I/SSU-B
      Effective QL: Opt-I/SSU-B, Priority: 255
  Next selection points: RP_SYSTEM RP_CLOCK_INTF
```

Investigates issues within individual interfaces. If the clock interface is down, a reason is displayed. This may be because there is missing or conflicting platform configuration on the clock interface.

Step 4 **show processes fsyncmgr location** *node-id*

Example:

```
RP/0/RSP0/CPU0:router# show processes fsyncmgr location 0/0/CPU0
```

```
                Job Id: 134
                   PID: 30202
       Executable path: /pkg/bin/fsyncmgr
            Instance #: 1
            Version ID: 00.00.0000
               Respawn: ON
         Respawn count: 1
Max. spawns per minute: 12
          Last started: Mon Mar  9 16:30:43 2009
         Process state: Run
         Package state: Normal
     Started on config: cfg/gl/freqsync/g/a/enable
                  core: MAINMEM
              Max. core: 0
              Placement: None
           startup_path: /pkg/startup/fsyncmgr.startup
                 Ready: 0.133s
      Process cpu time: 1730768.741 user, -133848.-361 kernel, 1596920.380 total
--------------------------------------------------------------------------------
```

Verifies that the fsyncmgr process is running on the appropriate nodes.

Class C Timing Support

To Configure Class C mode, see Class C Timing Mode.