Timing and Synchronization on Cisco ONS 15454

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Introduction

This document provides guidelines to plan the timing and synchronization on Cisco ONS 15454.

Prerequisites

Requirements

Cisco recommends that you have knowledge of these topics:

- Cisco ONS 15454

Components Used

The information in this document is based on these software and hardware versions:

- Cisco ONS 15454

The information in this document was created from the devices in a specific lab environment. All of the devices used in this document started with a cleared (default) configuration. If your network is live, make sure that you understand the potential impact of any command.

Conventions

Refer to Cisco Technical Tips Conventions for more information on document conventions.

Background Information

The product contains:

- The American National Standards Institute/Synchronous Optical NETwork (ANSI/SONET) provisioning platform
- The European Telecommunication Standards Institute/International Telecommunications Union/Synchronous Digital Hierarchy (ETSI/ITU/SDH) provisioning platform
- The transport platform, Dense Wavelength Division Multiplexing (DWDM)

The timing information in this document applies to the two provisioning platforms. The transport platform uses through timing. In through timing, the received east signal times the transmitted west signal, and the received west signal times the transmitted east signal.

Timing Architecture

The Timing, Communications and Control (TCC) cards and the cross connect (XC) cards control the timing function on the ONS 15454 based on industry standards for SONET/SDH equipment. Use redundant TCC and XC cards to provide fault tolerant common system hardware.

Note: This document uses TCC generically to refer to all variations of the TCC card, and XC generically to refer to all variations of the XC card.

The ANSI chassis contains two Building Integrated Timing Supply (BITS) In ports. Both ports terminate in the Auxiliary Interface Protection (AIP). The termination in the AIP allows both the active and standby TCC cards to monitor the BITS, and ensures proper termination of BITS even if the backplane is damaged due to a power surge. For the ETSI platform, BITS interfaces are located at the Front Mount Electrical Connection (FMEC) panel.

All synchronous interfaces (optical ports) derive the transmit timing from the system timing reference that TCC card manages. The XC cards provide transmit timing to each port. TCC performs these synchronization functions:

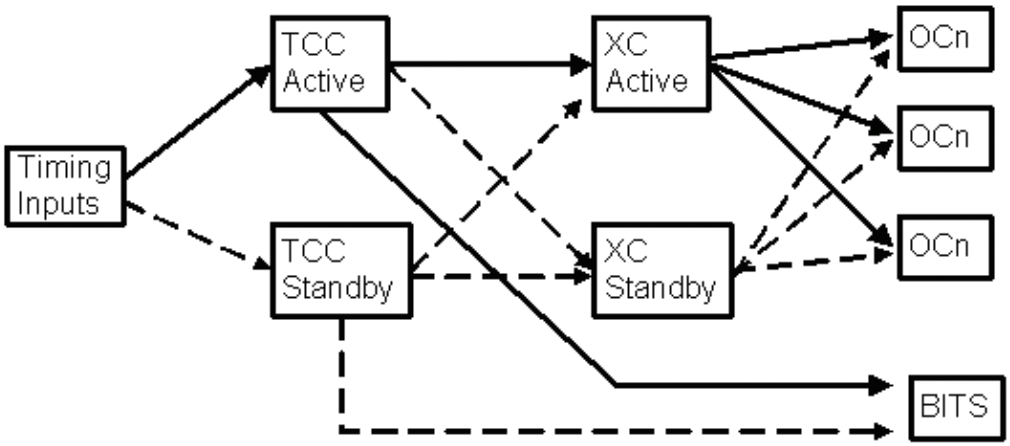
- To monitor, qualify and select reference.
- To filter and lock to the active reference.
- To manage the distribution of the system clock.
- To terminate two BITS inputs.
- To generate two BITS outputs.
- To process and generate synchronization status messaging (SSM).
- To switch reference for maintenance.
- To generate synchronization alarm reports.

Timing Distribution

Figure 1 indicates how timing is distributed within an ANSI system. The SDH version is similar but with minor terminology changes. This section uses the ANSI version as an example.

Note: The solid lines represent the active timing distribution, and dashed lines represent the standby timing distribution.

Figure 1 Timing Selection and Distribution in ONS 15454 ANSI



Each system can take multiple forms of inputs or reference clocks, on the basis of the timing provisioning. The available timing inputs are BITS 1 and 2, optical lines, and the internal oscillator. All these inputs are fed to both TCC cards though only the timing from the active TCC card is used. You can use provisioning to designate up to three inputs as reference clocks. The timing circuitry within each TCC card independently qualifies and selects one active reference among the three references and locks onto that reference. The resultant clock is called the system clock or NE clock.

Note: Both TCC cards do not lock onto each other.

The system clock from each TCC card is distributed to both XC cards, which feed the clock into all the OCn cards. The clock from the active XC card is selected.

Note: On SDH platforms, timing is distributed from the TCC cards directly to line cards over an internal bus.

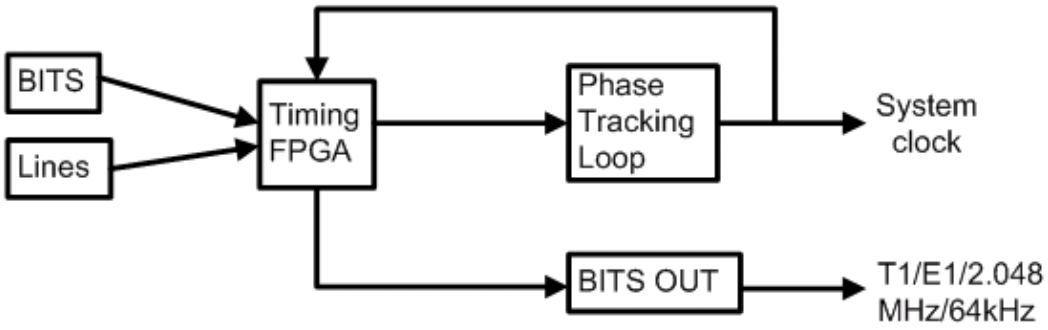
In order to drive other clocks, TCC cards can also generate BITS clocks from the lines.

Note: BITS Out clocks cannot be directly derived from BITS In clocks to prevent BITS timing loops.

Timing Circuitry

The timing circuitry in TCC cards handles all the timing related functions. Figure 2 shows a high−level flow. In order to determine the integrity, Timing Field Programmable Gate Array (FPGA) processes the timing inputs. The system clock is used as a reference for the comparison. The selected active reference is fed into the Phase Tracking Loop, which produces the system clock (NE clock). BITS signals can also be generated for signals that come from lines to provide timing to external devices (BITS Out). BITS Out ports provide two metallic interfaces that support a variety of signals.

Figure 2 Timing Circuitry in TCC



Reference Qualification and Failure

There are two ways to influence the selection of the active reference:

- Provisioning
- Reference qualification

Only the provisioned reference clocks are candidates for the selection process. One exception is the internal clock, which is always the default clock when all other references fail. However, a provisioned reference is not necessarily selected as the active reference. Any selected reference must pass the qualification process.

Each reference is polled every five milliseconds for state changes. Over a 30−second period, TCC computes frequency and wander for each reference. A reference is qualified (for acceptance) when the frequency offset is within ± 12.9 ppm. A reference is marked bad (rejected) when the frequency is outside of the valid frequency bounds (± 15 ppm for active BITS, ± 16 ppm for active lines, and ± 13.1 ppm for non−active references) and wander is beyond the threshold (2 ppm). A reference is also marked bad when an alarm is received, or if there is no signal. The alarm can be Loss of Signal (LOS), Loss of Frame (LOF) or Alarm Indication Signal (AIS). Failure of the active reference prompts the selection of and switching to the next best reference.

An IO card provisioned to provide line synchronization reference constantly monitors its received signal. If the port is in an LOS, LOF, or AIS state, the card turns off the reference to TCC. As a result, TCC declares the reference from the port as bad. If this reference is the current active reference, the next best reference becomes the active reference.

If an incoming clock has SSM associated with it, SSM is used for reference selection. The highest quality clock, whether or not SSM is used, is always selected as the active clock. When there are more than one references that have the same quality, the one with the highest priority (based on provisioning) is selected as the active reference.

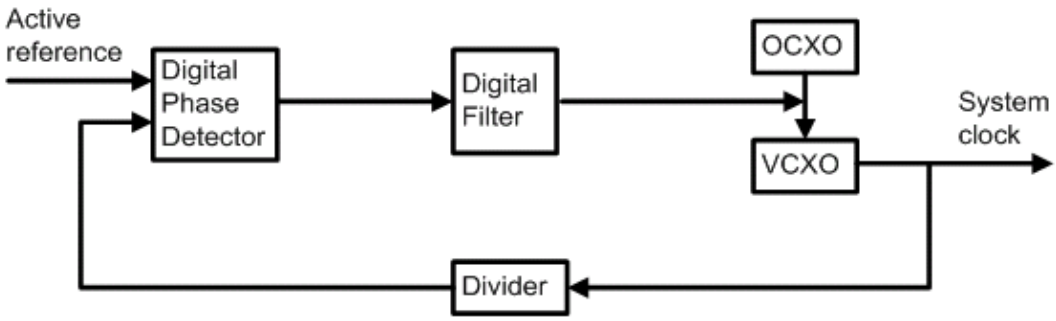
In summary, a reference is not accepted if any of these conditions is true:

- The optical or BITS input receives an LOS, LOF, or AIS alarm, or the interface is out of service.
- The SSM is in the do−not−use (DUS) state, or the SSM indicates the clock is of lower quality (in other words, the SSM quality of the reference is worse than that of TCC).
- The input frequency is off by more than ± 15 ppm for BITS or ± 16 ppm for lines over a 30−second period (out of bounds).
- The input clock is unstable (which means that the clock wanders at more than 2 ppm).
- It is not qualified for at least 30 seconds.

Phase Locked Loop

At the heart of the timing circuitry in TCC lies the clock generator block generated by the phase−locked−loop (PLL). Figure 3 represents a simplified PLL on TCC.

Figure 3 Phase Locked Loop



The phase detector compares the active reference clock with the system clock (already divided through the divider). If there is a phase offset, a voltage level proportional to the offset is generated. If there is no offset, no output is generated. The filter smoothes out or averages the voltage signal over some period, and feeds the average into the Voltage Controlled Crystal Oscillator (VCXO). The voltage adjusts the phase and frequency of VCXO. The output of VCXO is system clock (or NE clock). Part of the output is fed back into the loop to repeat the process. When the system clock tracks the active reference, the clock is locked and TCC enters the Normal clock mode.

VCXO is further stabilized by a smaller PLL between Oven Controlled Crystal Oscillator (OCXO) and the filtered reference clock.

Note: In order to simplify the diagram, this smaller PLL is not shown here.

The result is that the system clock is more stable. Notice that the OCXO used in TCC is rated at Stratum 3 for its holdover stability and free−run accuracy.

Card Level Synchronization Support

Optical Cards

- The system clock times all SONET transmit interfaces.
- Use pointer adjustments to resolve differences between input and output timing.

DS1/DS3 Cards

- The original DSx input rate determines the data rate of the output. The data rate is completely independent of the NE clock for the through timing mode.
- Use stuff bits at the initial mapping and pointer adjustments in the SONET network to resolve differences between the NE rate and the data rate.

DS3XM Cards

- The output line rate is locked to the NE clock.
- Individual DS1s within the DS3 retain their input frequency.

Timing Modes

ONS 15454 supports these timing modes:

- External
- Line
- Mixed

TCC cards have an internal Stratum 3 clock available to provide Holdover and Free−running timing support.

Note: Through timing and per−port loop timing are additional timing modes. However, ONS 15454 provisioning platforms do not support these modes.

Note: Electrical asynchronous interfaces are through−timed and do not reference the system timing. For these asynchronous ports, transmit timing is derived from the received timing for that asynchronous signal.

External Timing

This mode derives timing from an external timing device, for example, BITS or timing DS−1/E1. The quality level of the external timing device is better than the internal Stratum 3 clock.

Line Timing

Line timing derives the timing reference from one or more optical interfaces. Optical cards with multiple optical interfaces can only provision one interface as a timing reference port. The incoming recovered clock is converted to a 19.44MHz signal, transmitted to the TCC cards and qualified as a timing reference. In Line timing mode, available timing references are optical interfaces and the internal clock.

Note: When optical ports are provisioned as 1+1, only the working port is provisioned as a timing reference. The protection port is automatically selected during a switch over.

Mixed Timing

Mixed mode timing allows both External (BITS1/BITS2) and Line (optical interfaces) timing references to be selected as well as the internal clock. Be careful when you use Mixed mode timing, because timing loops can easily occur. Therefore, plan carefully before you use Mixed mode timing. Alternatively, use looped BITS.

Clock Modes

Normal Mode

In the Normal operation mode, TCC is locked onto an external timing source.

Fast−start Mode

An oscillator uses the Fast−start mode for fast pull−in of a reference clock whose frequency is far apart from that of the oscillator. Fast−start is sometimes referred to as the Acquire State . If TCC changes to a reference that is close to the rate at which the TCC card already runs, the mode directly changes to Normal.

Holdover Mode

In the Holdover mode, all external or line timing references are lost and the clock uses timing data referenced while in normal operating mode to control its output signal. However, holdover frequency drifts over time until a timing reference becomes available. If the previous timing reference was available for less than 140 seconds before it was lost, TCC enters the Free−running mode when the timing reference is lost.

This mode is better than the Free−running mode because it uses the average of 140 seconds of data from the last qualified timing reference to augment its internal clock. TCC remains in this mode until a reference becomes available to switch or the drift is out of bounds. Traffic is guaranteed to be uninterrupted by a transition to the Holdover mode for the first 24 hours.

Free−running Mode

Free−running mode only references the internal clock on the TCC card. This mode is also the default mode when other references are lost, even when it is not specifically provisioned as a reference. Ensure that your network does not operate with the internal clock of the TCC card as the only or primary timing source.

Guidelines to Plan Synchronization

Features of Good Timing Design

Good timing design:

- Incorporates a logical timing hierarchy.
- Provides efficient synchronization.
- Avoids timing loops.
- Recovers from timing failures quickly.

It is always best to have redundant and accurate external timing sources for a network larger than a few nodes. In real networks, this is not always possible or required.

Internal timing is not intended for use as the primary timing source during normal operation. Cisco recommends that you use a higher quality source (preferably Primary Reference Source/Primary Reference Clock (PRS/PRC) clocks) for primary network timing with the internal clock available for times when all other timing sources fail.

For high traceability, minimize the number of ONS 15454 nodes line timed in a daisy−chain fashion from a master node. As a general guideline, you can have up to seven nodes for the primary direction and 13 nodes for the secondary direction. Carefully plan line timing in a ring in order to avoid timing loops.

Timing loops can cause large frequency errors as the node tries to track its own clock, which in turn can result in ONS 15454 nodes to repeatedly enter Holdover, Fast−start, or Free−run timing modes. Often there is no alarm to indicate that a timing loop exists.

Related Information

- **Technical Support & Documentation − Cisco Systems**

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